Analysis of the EU International Cooperation Opportunities

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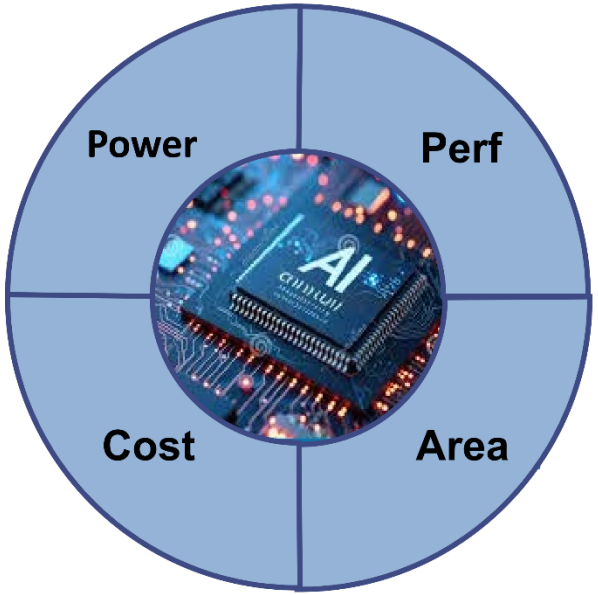
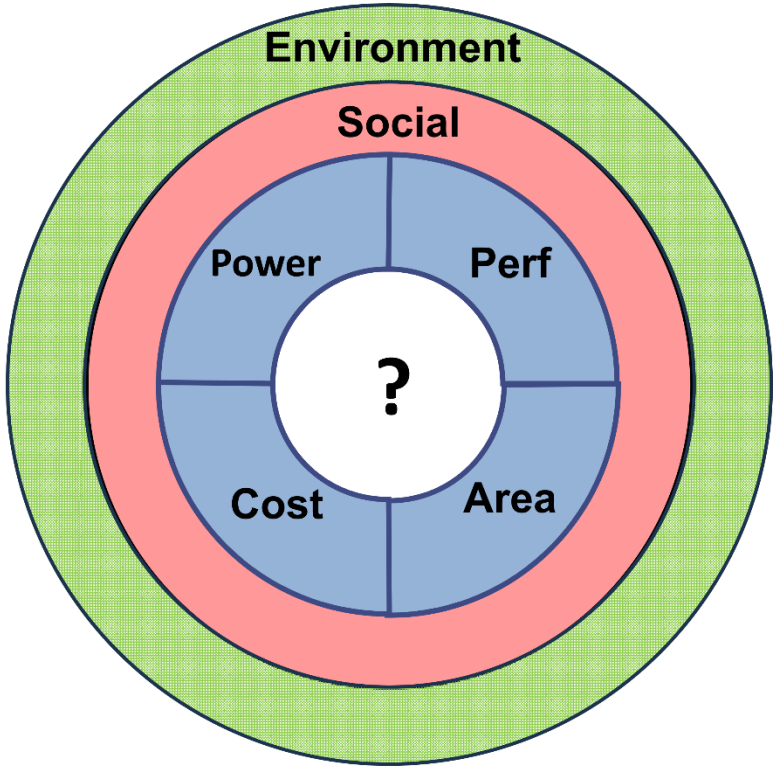
What are we aiming for?

Today's Drivers
Performance & economy



PPAC

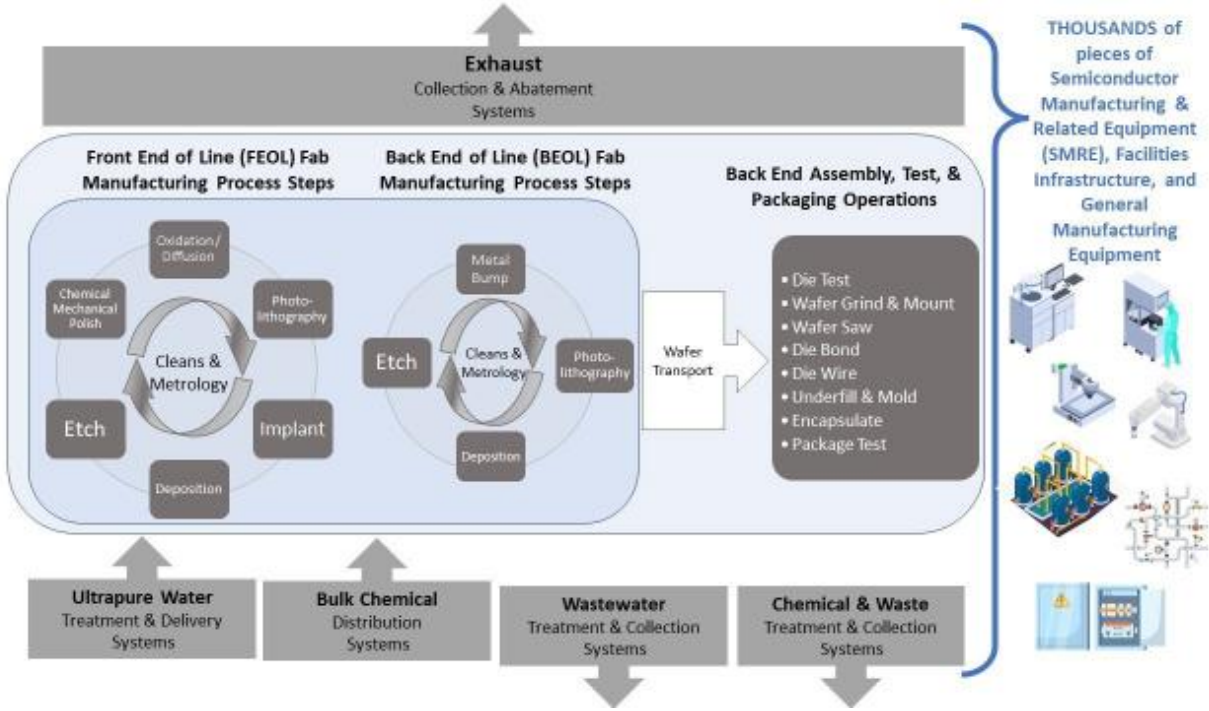
Tomorrow's Drivers?

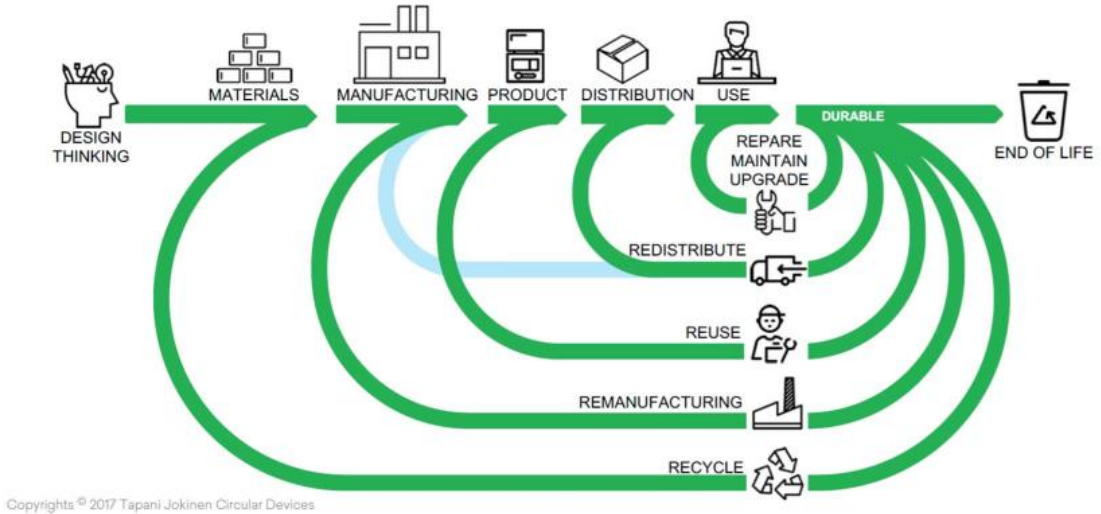


PPAC – E & S

Source: Jean-Pierre Raskin (UCL, Université Catholique de Louvain)

Environmental and social impact

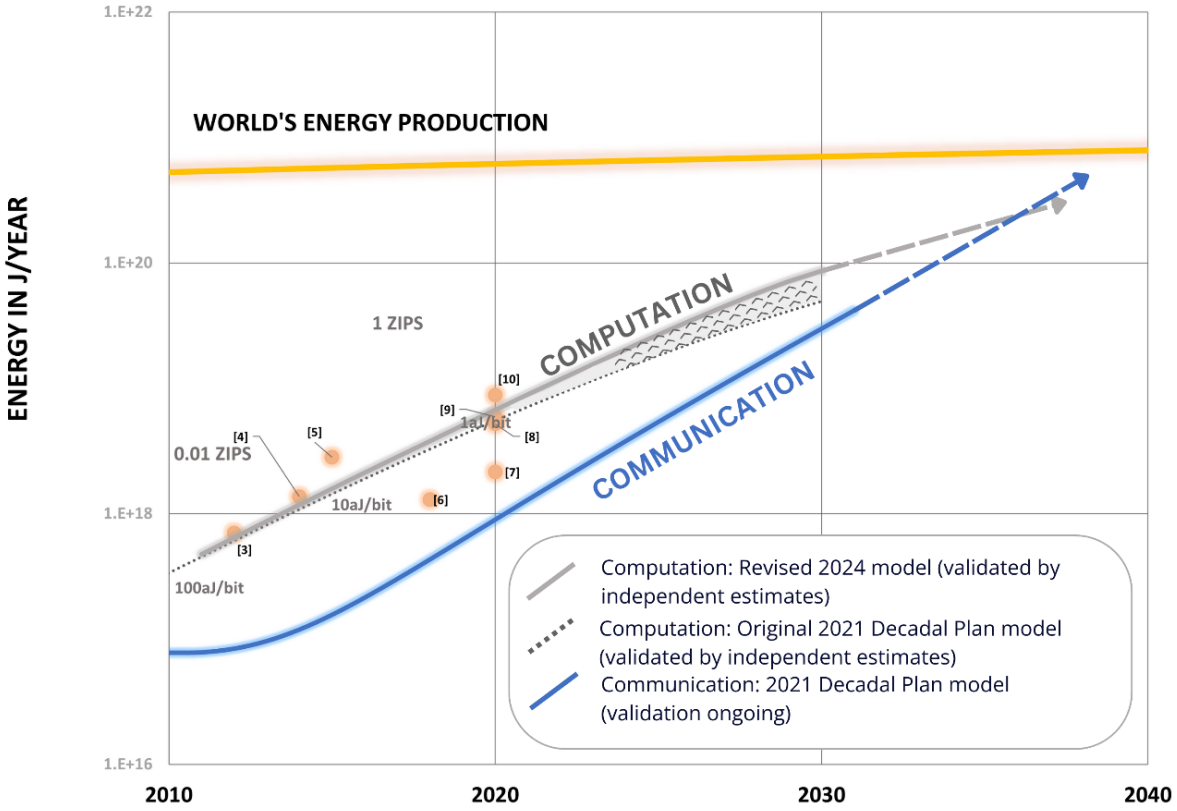




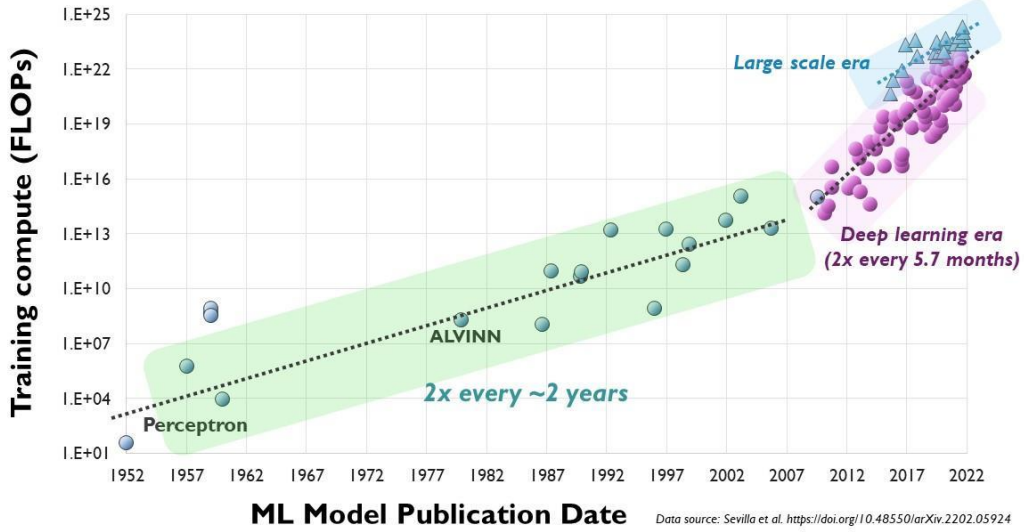
- **Sustainability** of semiconductor manufacturing (fluorinated organic chemicals, PFAS, throughout the process)
- DfM (Manufacturability) -> DfT (Testing) -> DfR (Reliability) -> **DfC (Circularity)**

Source: RINA Tech UK Limited (SIA PFAS Consortium); Tapani Jokinen Circular Devices

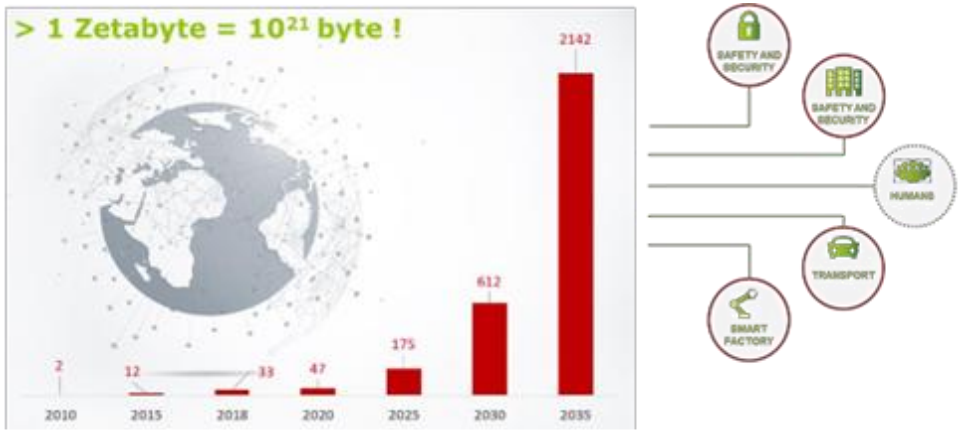
Advanced computing trends



Global power wall



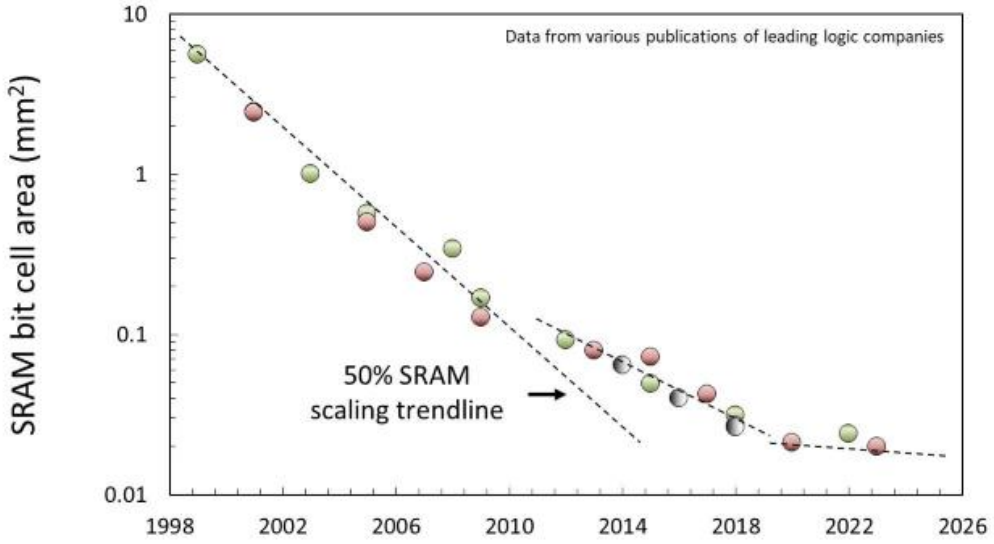
Computation needs (ML)



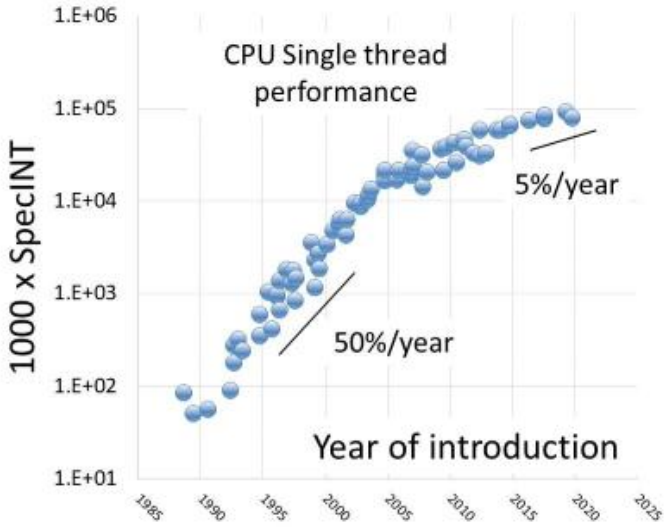
Global data generation

Source: RINA Semiconductor Research Corporation; Nadine Collaert (imec), Olivier Faynot (CEA- leti)

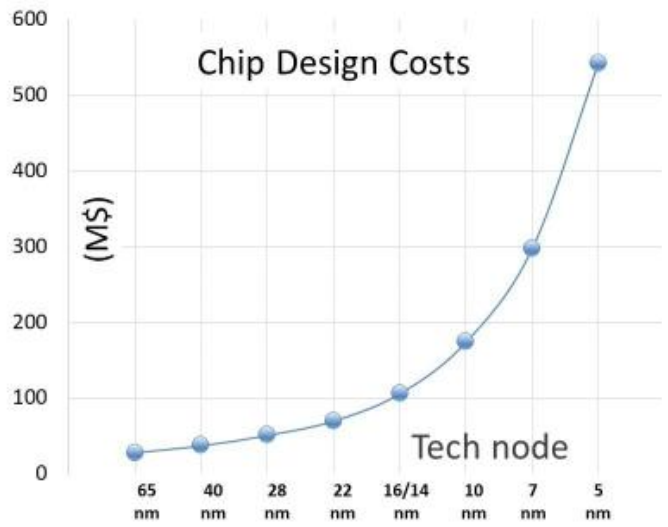
Area-Performance-Cost challenges



SRAM size
as function of introduction year



CPU performance
as function of introduction year



Design costs
as function of CMOS node

- **Memory wall**: growing disparity between processor speed and memory performance
- **Power wall**: challenge of improving performance without a proportional increase in power consumption

Source: Nadine Collaert (imec), Olivier Faynot (CEA- leti)

Diversity of applications and workloads

GPUs for Training

High throughput parallel compute

Very high memory bandwidth

Very high GPU-GPU bandwidth

AR/VR

Low power

Ultra low latency

High memory bandwidth

Small form factor

Autonomous driving

Multi-sensor fusion

Distributed real-time computation

Reliable and explainable AI

Key challenge: a **“one size fits all” approach is not possible** due to the myriad of diverse “advanced computing” needs

Source: Nadine Collaert (imec)

Diversity of applications and functionality

ubiquitous intelligence

Analog (real-time) measurements

Ultra low latency

Fusion of sensor data
'Edge' data processing

Cost/Economics

Energy autonomy of devices

Secure and reliable data

Reliability and life-cycle

Environmental sustainability

Medical - Highly sterile

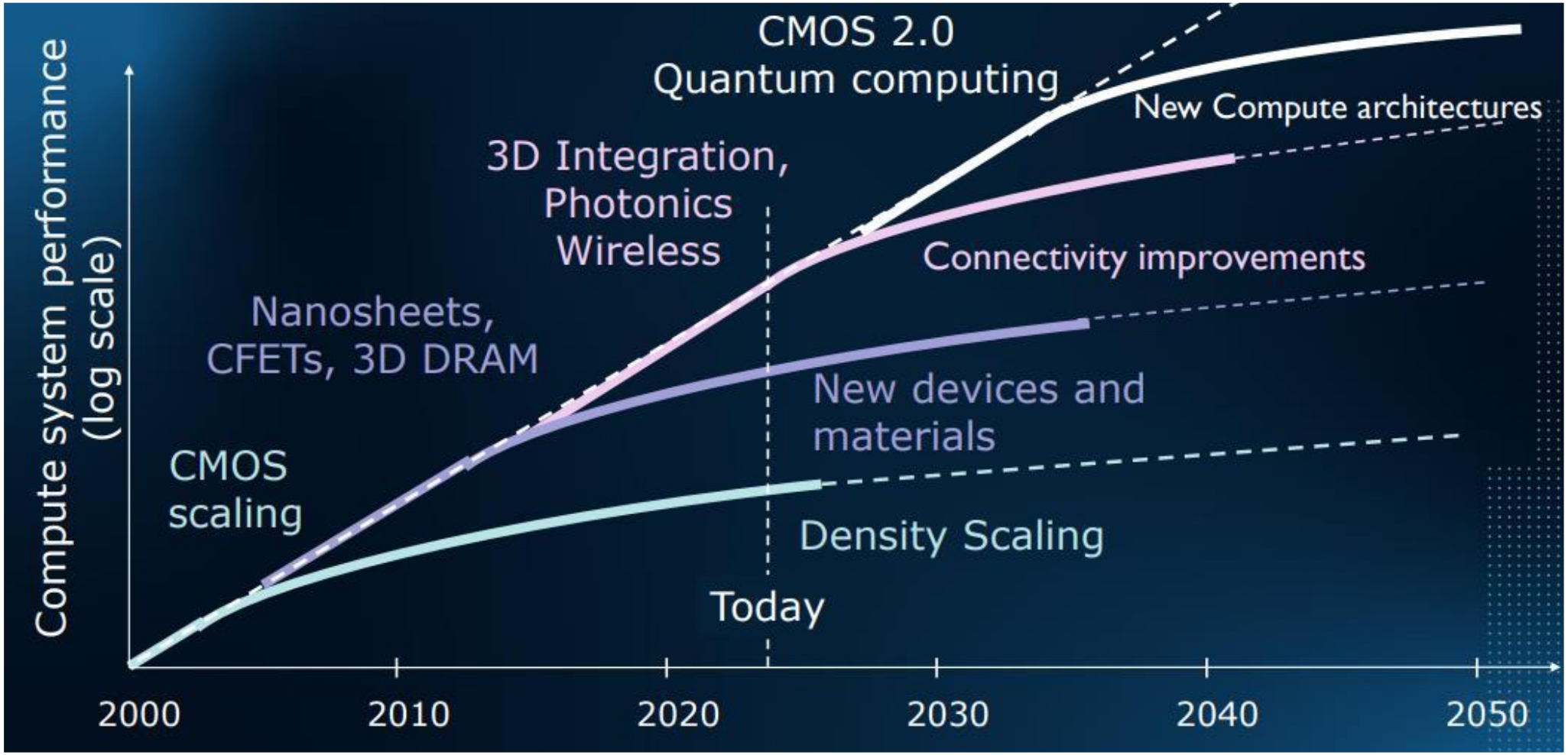
Automotive - Temperature

On-Farm - Fouling

Key challenge: a **"one size fits all" approach is not possible** due to the myriad of different deployment scenarios

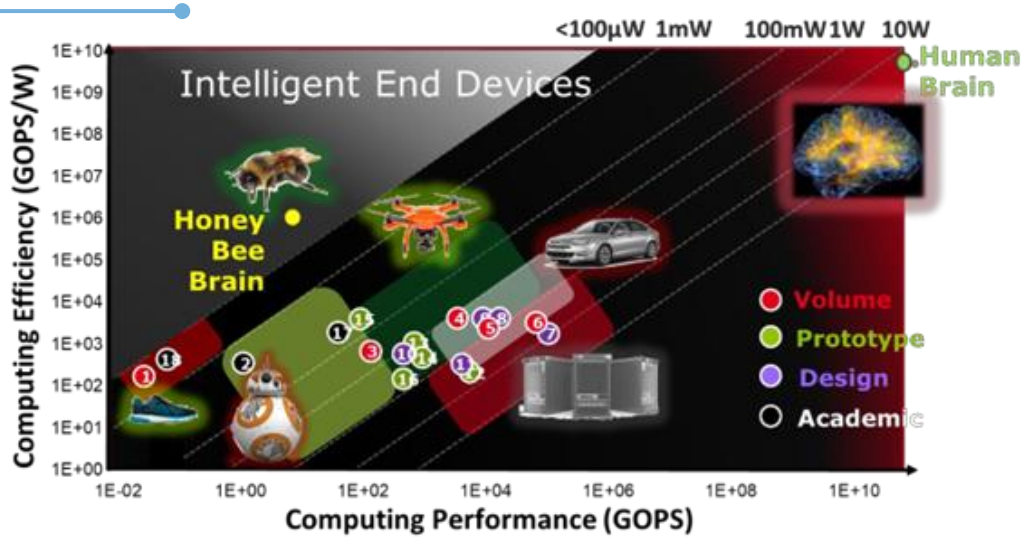
Source: Giorgos Fagas (Tyndall National Institute)

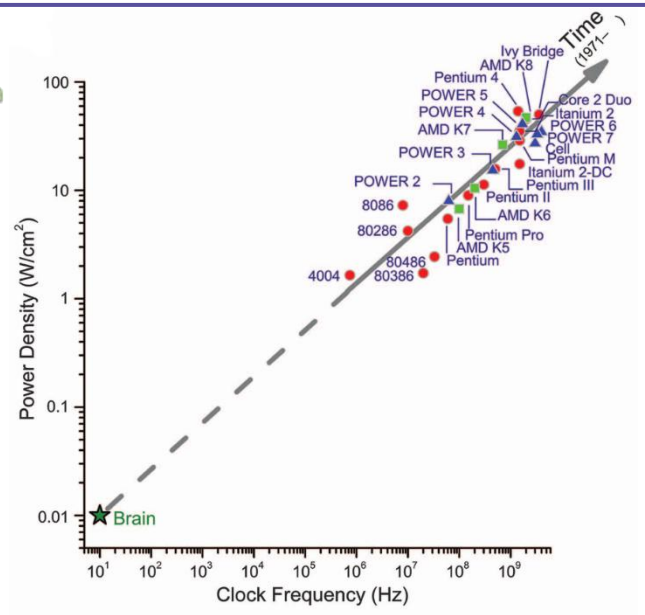
Technology boosters for future compute

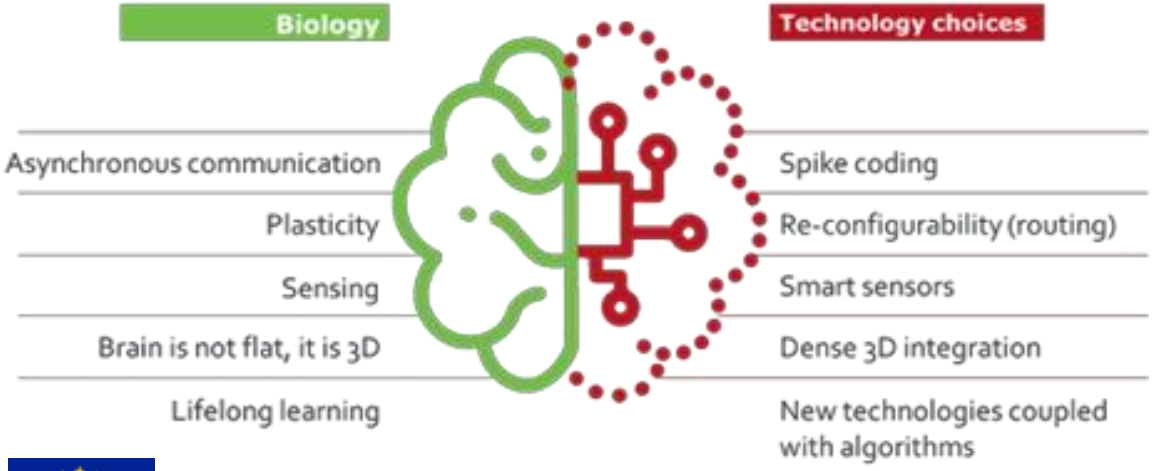


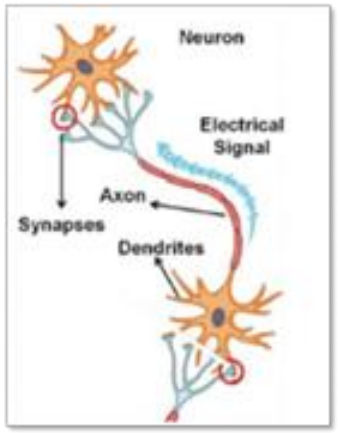
Source: Giorgos Fagas (Tyndall National Institute)

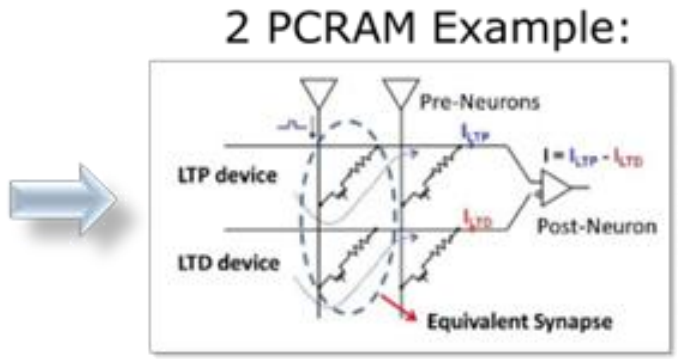
Nature is a great engineer





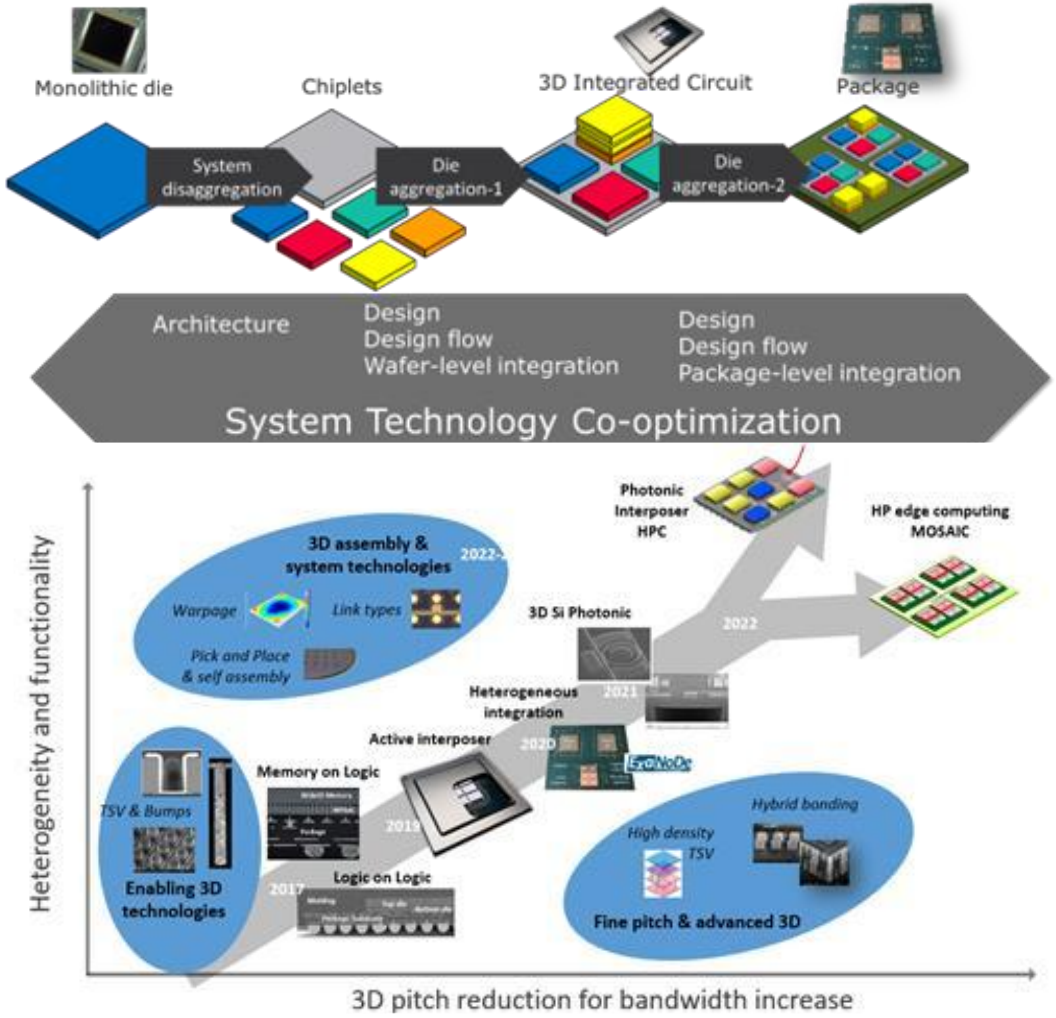


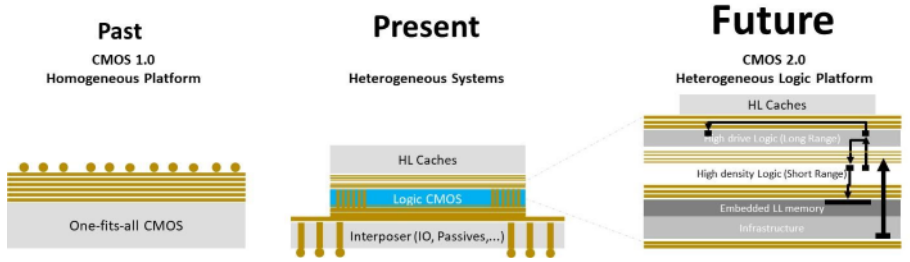


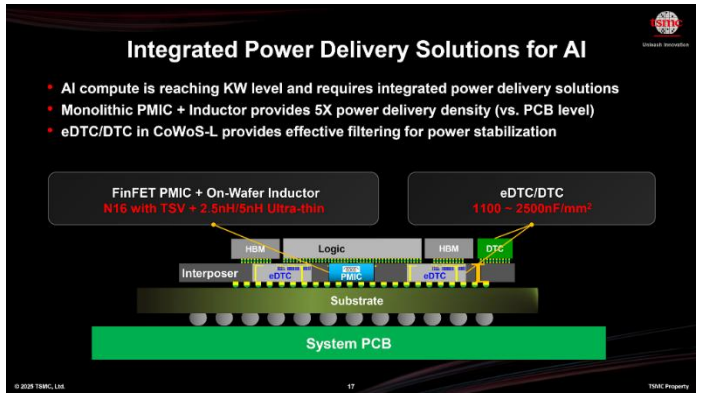


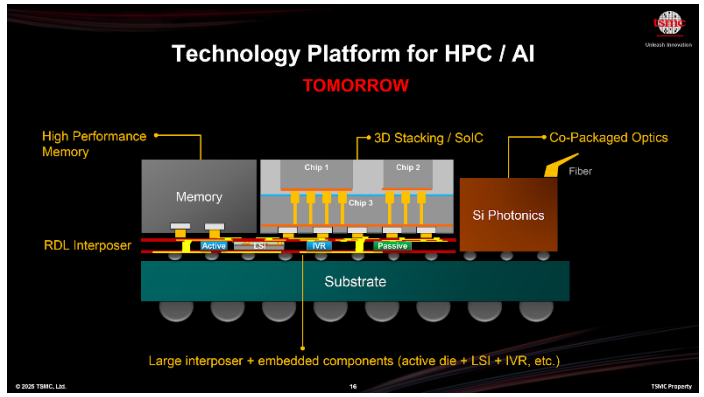
Source: Nadine Collaert (imec), Olivier Faynot (CEA- leti); IBM Research

CMOS 2.0: system scaling





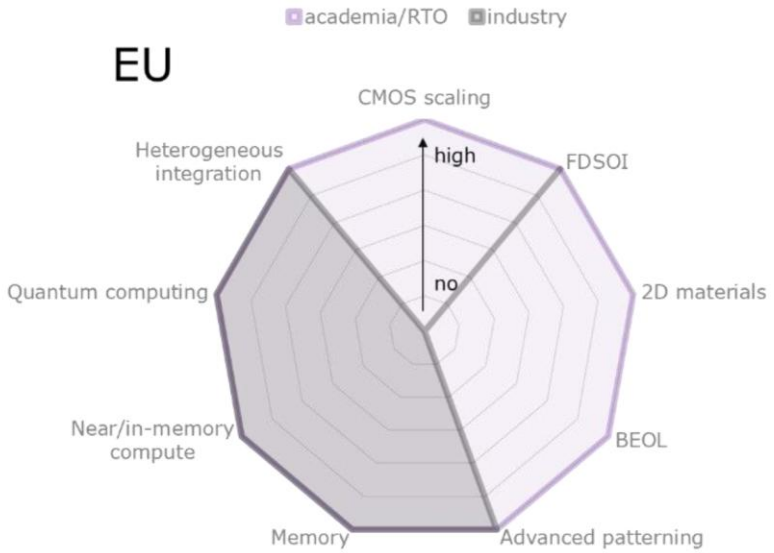


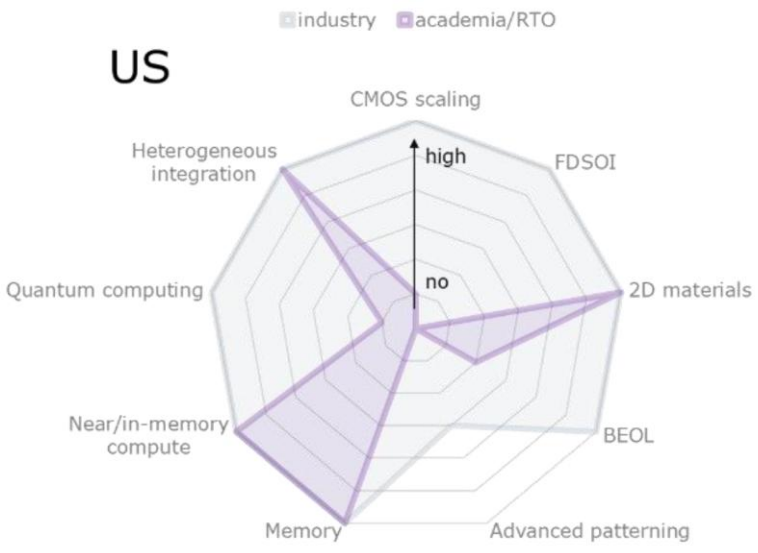


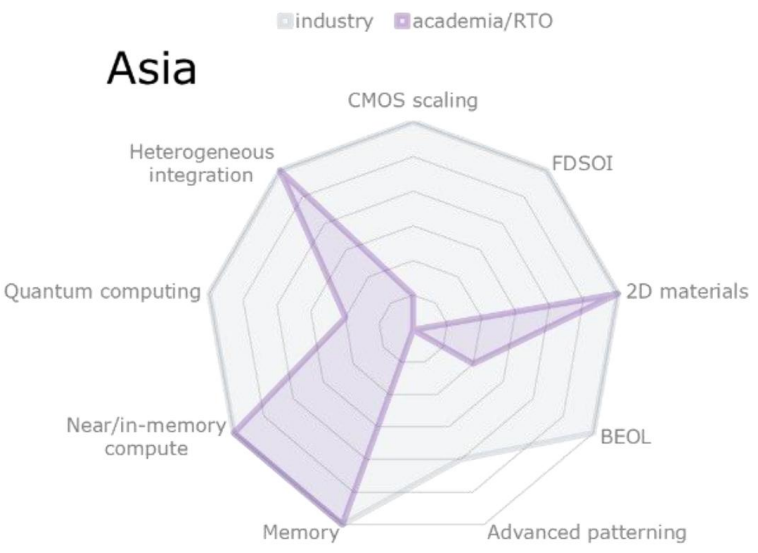
- System-technology co-optimization
- Moore's law 2.0: more functionality per unit area
- Smart disintegration to re-integration

Source: Nadine Collaert (imec), Olivier Faynot (CEA- leti), TSMC

Actors in the field of advanced computing







- EU: very strong in all R&D domains; weak in advanced materials and CMOS technologies manufacturing
- US and ASIA (similar profiles): stronger in manufacturing than in R&D

Source: Nadine Collaert (imec), Olivier Faynot (CEA- leti)

EU - Non-EU Cooperation Opportunities

Investigation and evaluation methodology

Goal: For each country, identify strengths and weaknesses.

Across the value chain:

- Logic
- Memory
- Mixed-signal processing
- Powering
- Sensing
- Communication
- Photonics

Through the value chain:

- EDA & IP
- Chip Design
- System Design
- Materials Integration
- Components
- Manufacturing (front-end)
- Manufacturing (back-end)
- Equipment & Tools (front-end)
- Equipment & Tools (back-end)

Radar maps:

- Scores from 1 to 5 (-1 if not enough data)

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Survey for non-EU strengths/weaknesses

Who should be invited:

- Any expert in the interested research fields from the target countries.
- Any expert in the interested research fields with a solid experience in the target countries.

What to focus on:

- Strengths & weaknesses.
- Challenges & opportunities.

Target countries:

- USA
- Japan
- Republic of Korea
- China
- Taiwan
- Singapore
- India

« Considering your field of expertise, …, for each segment of the value chain … »

Rate the overall strength of the target country

- See Deliverable D3.3 "Recommendations for International Research Cooperation" for suggested international cooperation topics
- Numerical scores
- Optional comments and suggestions

Source: deliverable D3.3 "Recommendations for International Research Cooperation"

Logic

- **AI-enhanced EDA tools** for optimizing, verifying and predict logic designs across power, performance, area, cost, security and sustainability.
- Brain-inspired **neuromorphic devices and architectures** for edge computing systems, requiring low latency and high energy efficiency, including AI at the edge.
- High-bandwidth logic subsystems optimized for interconnects in network-on-chip architectures.
- Research and development of **advanced transistor technologies** and related manufacturing processes for future generation of FinFETs, nanosheets and CFET transistors for sub-3 nm nodes, with novel device geometries.
- Development of components enabling neuromorphic computing and **quantum logic devices**.
- **New materials integration** for alternative channel materials and added back-end-of-line (BEOL) functionality.
- Substrate thinning processes and **back-side processing** for new power and backside passive and active functionalization.
- **Heterogeneous integration** at the core of design and manufacturing processes for integrating logic cores with accelerators and memories, based on optimized IPs, and using chiplets and 2.5D/3D packaging.

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Memory

- EDA solutions for **emerging memory technologies**, including reliability and performance modelling.
- IP design for **novel memory hierarchies** in data-centric computing, including persistent memory IPs for in-memory computing.
- Development of **logic-in-memory** designs to enable compute capabilities within memory chips.
- Designs for heterogeneous memory systems that optimize for workload-specific requirements (e.g., HPC, AI, IoT).
- System-level solutions for **memory integrity verification and protection** against data corruption and hacking, integrating advanced secure memory technologies for critical applications like autonomous vehicles and defence.
- Design and manufacturing of **components for in-memory computing**, including logic-in-memory approaches to reduce data movement and latency, exploring also FeRAM, MRAM, RRAM, phase-change memory and other storage-class memory solutions for hybrid memory/storage systems.
- Development of techniques for **testing** and mitigating failure mechanisms in stacked and hybrid memory architectures.

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Mixed-Signal Processing

- **Seamless integration** of the analog and digital design and development.
- **Heterogeneous simulation and modelling** approaches at different levels, considering also IP libraries.
- Development of **structural solutions for** mitigating and preventing critical **integration** issues.
- **Design for Testability**

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Powering

- **Tools and libraries** that support the design of systems in the specific area of power devices and power harvesting, including Design for Testability (DFT) and Design for Manufacturability (DFM), yield management, reliability/fault tolerance and aging analysis, integration and interoperability.
- Methods and **tools for integrating multiple components** (e.g., passives) into a cohesive system for better performance and efficiency and for reducing the size of components while maintaining or improving performance.
- Equipment for **quality control measures**, ensuring that products meet industry standards and specifications and implementing real-time monitoring systems to track performance and detect issues in manufacturing equipment.
- Wide band gap (e.g., SiC, GaN) and ultrawide band gap **materials** (e.g., AlN, GaOx, diamond) for power devices.
- Focusing on energy harvesting:
  - Development of **environmentally friendly materials** for energy harvesters.
  - Develop **comprehensive system design** including all process aspects for increasing power generation efficiency.
  - A general limitation towards industrial adoption of Energy Harvesting is its reliance on environmental conditions. Developing **Energy Harvesting combined with on-demand charging** of the device could help solving this issue.

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Sensing

- New approaches are required to facilitate integration of **sensor performance into traditional simulation** tools such as SPICE. This will enable seamless integration of the full sensor system.
- Key challenges remain around the **need to calibrate individual sensors**, ML methods at different levels are required to address these challenges.
- **Scaling up sensor functionalisation and characterisation** in-line with wafer-scale production.
- Developing of **safe and sustainable and design fabrication**, modification and characterisation.
- **Advanced sustainable (bio)materials** innovation and integration of in new, highly sensitive and more versatile sensors.

Communication

- **ML-enabled tools** for designing, optimizing, and integrating RF and mixed-signal circuits for 5G/6G applications, including system-level co-simulation of digital, analog, and RF components in heterogeneous systems.
- **New materials** for RF, mmWave and sub-THz devices, advanced dielectric materials and substrates for wireless/wireline applications and components.
- Innovations in the **co-integration of passives with active components** in heterogeneous systems, progress in antenna-on-chip and antenna-in-package technologies for high-frequency applications.
- Techniques to **scale RF technologies alongside digital nodes** while ensuring performance and reliability.

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Photonics

- **Tools** for photonic active and passive circuit design and photonic-electronic codesign, layout, and simulation, including IP libraries and across multiple technology platforms.
- **Heterogeneous and hybrid photonic-electronic integration platforms** including multi-chip modules/chiplet integration, integration of light sources, back-end and front-end heterogeneous integration, optical fiber coupling and package design.
- Development of PDKs, ADKs etc. for **rapid prototyping**, bypassing long chip iteration cycles
- High-volume pure-play **foundries** for photonic integrated circuits, **out-sources assembly and test** providers (OSAT).

Source: deliverable D3.3 “Recommendations for International Research Cooperation”

Warsaw Workshop

SESSION 3 – EU International Cooperation on Semiconductors: Opportunities and Challenges

- **Rakesh Kumar, Chair of IEEE Future Directions, DataPort, Past-chair IEEE Roadmaps, (USA)**
- **Yong Lian, IEEE Division 1 Director, member of the IEEE Board of Directors, (China and Singapore)**
- **Dr. Tuo-Hung Hou, Director General of the Taiwan Semiconductor Research Institute (TSRII), (Taiwan)**
  250513 ICOS_TSRI
- **Sunita Verm, Group Coordinator (R&D) at Ministry of Electronics & IT, (India)**
  Landscape of Indian Research and Development in Semiconductors
- **Jinwook Burm, Professor at Sogang University**
  Semiconductor Industry in Korea & EU International Cooperation on Semiconductorw
- **Hiroyuki Akinaga, University of Hokkaido / National Institute of Advanced Industrial Science and Technology (AIST)**

EU

How to collaborate:

- Ambitious roadmapping
- Co-funded joint R&D and Innovation
- Talent Development and Education
- Joint ventures including Public-Private partnerships
- Standardisation and Regulation

What to collaborate on:

Country	Key Benefit	Dependency Reduced On
USA	IP tools, R&D, design frameworks	US toolchain dominance (mitigated via joint development)
Taiwan	Advanced logic chips	Asian-centred high-end production
Japan	Raw materials, equipment	Chinese material exports
South Korea	Memory & logic fab diversity	Korea-only supply vulnerabilities
India	Design, backend, scaling workforce	China/Asia-centric labour + design

Source: Giorgos Fagas (Tyndall National Institute)

USA

Let’s focus on each Region’s Strengths to fill the Gaps

- Systems Architecture
- Design
- Process Technology
- Packaging
- Test
- …

- Spawn “Silicon valley-like” infrastructure for Start-ups

Source: Rakesh Kumar, Chair of IEEE Future Directions, DataPort, Past-chair IEEE Roadmaps, (USA)

China & Singapore

Collaboration Opportunities

EU strength:

- Semiconductor materials, equipment, design, manufacturing (mature nodes and power semiconductors)

Singapore strength:

- Strong government support
- Ideal environment for investment

China strength:

- Manufacturing capacity
- Packaging and testing
- Huge market
- Pool of manpower
- Significant opportunities for innovation

Areas for Collaboration:

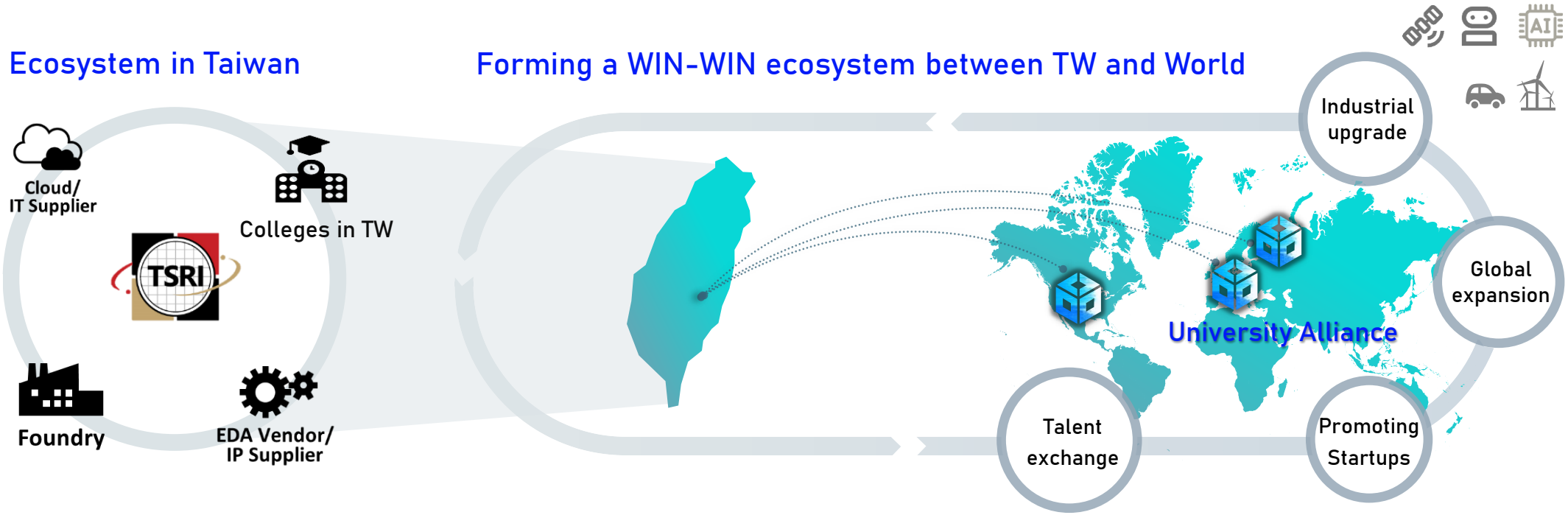
- Joint R&D in quantum computing AI chips, and emerging memory technologies
- Collaborating to integrate supply chains and technology platforms.

Source: Yong Lian, IEEE Division 1 Director, member of the IEEE Board of Directors, (China and Singapore)

Taiwan

From Silicon Valley to Taiwan, and now from Silicon Island to the World

Connecting Taiwan's semiconductor research and talent cultivation system to the world, and collaborating with likely-minded partners to jointly build a new **WIN-WIN** ecosystem



Source: Dr. Tuo-Hung Hou, Director General of the Taiwan Semiconductor Research Institute (TSRI), (Taiwan)

India

Best fields for cooperation

- Logic
  - Microprocessor (RISC-V), GPU and AI/ML accelerator and In-memory computing
- Mixed-signal processing
  - Wireless & RF SoC Technologies (i.e. RF front-end integration for 5G, Bluetooth, Wi-Fi, Mixed-signal support for software-defined radio (SDR), mmWave and sub-THz mixed-signal transceivers).
- Powering
  - Power management ICs, IGBTs required for EVs, HPCs & Power Electronics systems.
  - GaN and SiC based ICs and sub sytems for e-mobility applications.
  - SiC and GaN based converters/power electronics devices for energy systems.
- Sensing
  - Sensor technologies for IoT, Advanced Manufacturing and Smart City applications.
- Communication
  - Integrated Sensing and Communication
  - Next-G wireless network technology
  - AI-native design in wireless communication
- Photonics
  - Chip Interconnects
  - Photonics ICs

Source: Sunita Verm, Group Coordinator (R&D) at Ministry of Electronics & IT, (India)

Republic of Korea

International Cooperation

- EU Semiconductor
  - Strong in fundamental research & IPs
  - Strong in Equipment (ASML)
- International Programs
  - Cf. Sogang U. – AMSL program
- Research funds
  - Cf. International Technology Development in Semiconductor/Display (www.iris.go.kr)

- Korean Organizations
  - Korean Organizations (www.theise.org)
  - IEEE Circuits and Systems Society
  - Cf. Sogang U. – AMSL program
  - IEEE Solid-State Circuits Society
  - IEEE Solid-State Circuits Society

Source: Jinwook Burm, Professor at Sogang University (Republic of Korea)

Japan

Best field for cooperation

Logic, memory, mixed-signal processing, powering, sensing communications, photonics… **Difficult to choose "Best"**

Most challenging sectors for cooperation

Materials integration: The impact of material integration is significant, but it must be Green.

Recommendations for research cooperation

Development of a method to evaluate the **environmental impact** of introducing new materials **using digital twins**.

Source: Hiroyuki Akinaga, University of Hokkaido / National Institute of Advanced Industrial Science and Technology (AIST) (Japan)

THANK YOU FOR YOUR ATTENTION

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